REMARKS

The Office Action of May 11, 2004, has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested.

Claims 47-67 remain in this application.

Claims 56-58 have been amended to clarify the language of the claims. Claim 56 has replaced "data circuit" with "latch circuit" to correct its identification. Claims 57-58 have been amended to more clearly identify the memory cell arrays (changing "third memory cells" to "second memory cells" to remove any question regarding the existence of "second memory cells"). These are not narrowing amendments. The scope of the claims is the same as before. No new matter has been entered.

Claims 47-67 stand rejected under 35 U.S.C. 102(a) over Hemink et al. Applicants strenuously traverse.

Claim 47, as amended, recites, *inter alia*:

> " a first signal line connected to said first memory cell section;
>
> a second signal line connected to said second memory cell
>
> section, being different from said first signal line; ... "

In contrast, according to Hemink et al., the first and second signal lines, which the Examiner indicated, are in fact the same line. They are electrically shorted together. With this structure, Hemink et al. cannot realize the action that data of a first memory cell is latched in a latch circuit while data of a second memory cell is held by the second signal line.

In the May 11, 2004, office action, the Examiner now points to the SRC lines of the memory cell arrays of Figure 8 to show a first signal line and a second signal line being different from each other. Hemink does not disclose the operation of the first and second signal lines as claimed. The structure of Figure 13 does not disclose "first program /read data of said first memory cell is latched in said latch circuit, while second program /read data of said second memory cell is held by said second signal line."

The other independent claims and dependent claims are allowable for similar reasons.

Claims 46-47 stand rejected under 35 USC 102(e) over Sakui et al. Applicants traverse.

Figure 38 of Sakui et al. does not relate to the recitations of claims 46-47. Column 33, lines 27-39 of Sakui et al. indicate that the data circuit of Figure 38 relates to storing data in pairs.

> " FIG. 38 shows an arrangement using a differential sense amplifier. In this case, 1-bit data may be stored in two memory cell units as complementary data. Data is read by detecting a small difference between signal amounts (potentials) output from the two memory cell units and amplifying this difference. This allows a high-speed read.
>
> One-bit data is stored in a pair of memory cell units. For this reason, even when the program/erase endurance characteristics of one memory cell unit degrade due to the repeated data change operation, the reliability does not decrease as far as the other memory cell unit has satisfactory program/erase endurance characteristics."

Both the left and right side memory cells are accessed in parallel using BLi and /BLi. In other words, they operate the same way at the same time. This is different from the recitations of claim 47 and 48. Accordingly, these claims are allowable over Sakui et al.

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It is believed that no fee above the extension of time fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733 accordingly. No additional claim fees are believed due. If any fees are due, the Commissioner is authorized to debit our deposit account no. 19-0733.

Respectfully Submitted,

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$1,750.00

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